WHAT IS CLAIMED IS:

1. A digital camera, comprising:

an image sensor having a first resolution;

a timing generator for reading a first resolution image signal from said image sensor;

a first processor for performing predetermined signal processing on said first resolution image signal;

a thinning-out circuit for thinning out said first resolution image signal outputted from said first processor and creating a second resolution image signal with a resolution lower than said first resolution;

a main memory having at least two memory areas;

a selector for selecting alternately said two memory areas;

a write controller for writing said second resolution image signal to one of said two memory areas based on an output of said selector; and

a read controller for reading a second resolution image signal from the other of said two memory areas based on an output of said selector.

2. A digital camera according to claim 1, wherein said timing generator reads out said first resolution image signal in an amount of one screen at an interval of a first predetermined period, and said read controller reading out said second resolution image signal in an amount of one screen at an interval of a second predetermined period shorter than said first predetermined period.

3. A digital camera according to claim 2, wherein said second predetermined period is 1/Nth (N is an integer equal to or greater than 2) of said first predetermined period.

4. A digital camera according to claim 2, wherein said selector alternately

switches for a memory area to be selected at an interval of said first predetermined period.

5. A digital camera according to claim 1, further comprising a monitor to display an image corresponding to an image signal read by said read controller.

6. A digital camera according to claim 1, further comprising:

an instruction key; and

a second processor for outputting at predetermined timing a first disable signal, a second disable signal and a third disable signal in response to operation of said instruction key; wherein

said thinning-out circuit being disabled by said first disable signal simultaneously with the operation of said instruction key,

said read controller being disabled by said second disable signal simultaneously with the operation of said instruction key, and

said write controller writing said first resolution image signal outputted from said first processor to said main memory and disabled by said third disable signal after said first resolution image signal in an amount of one screen has been written.

7. A digital camera according to claim 6, further comprising a recorder to record said first resolution image signal written on said main memory to a recording medium.

8. A digital camera according to claim 7, wherein said second processor cancels said second disable signal from outputting after said first resolution image signal has been recorded, and said read controller reading said first resolution image signal from said main memory.

9. A digital camera according to claim 1, wherein said memory has a single signal input/output port.